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Review of multicrystalline silicon wafer solar cell processing

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Abstract

The challenges for searching and utilizing of new and sustainable energy sources especially solar cell electricity. The major obstacle of using solar cells for electricity generation has been a much higher price when compared to the price of electricity generated from the traditional sources. The photovoltaic industry needs to put an enormous pressure and optimization at every stage of the photovoltaic manufacturing chain of multicrystalline silicon wafer solar cell processing in order to reduce cost. Processing of multicrystalline silicon solar cells is starting by silicon wafer preparation, etching and texturing, saw damage etching, surface texturing, phosphor diffusion & edge isolation, phosphor diffusion, edge isolation, silicon nitride deposition for antireflection coating, and metallization process that consist of screen printing ag front side, screen printing of al back side, drying and firing and formation al back surface contact. Mechanical stability of silicon wafer became a serious issue due to reduction of wafer thickness, so probability for wafer to breakage is high; investigate the mechanism of wafer breakage is important to reduce breakage. The present of micro cracks reduces the mechanical strength of wafer significantly and wafer breakage will increase, because crack will start from the existing micro crack and that will propagate easier with presence of the stress. Mechanical stability is increase significantly after the etching process; on the other hand the screen printing process will reduce wafer strength. Etching of saw damage, that is induced during wafer slicing, and metallization of the surfaces are 2 crucial processing steps in the manufacturing of mc-silicon solar cells.

Keywords: Solar cell energy, photovoltaic, silicon wafer, multicristalline, processing step, wafer breakage**.**

1. Introduction

1.1. Background

A new challenge has emerged at the end of the 20th century that represents a search for and a utilization of new and sustainable energy sources. The urge of this challenge is underlined by limited resources of the fossil fuels on the Earth and increasing demand for energy production. This is the reason why the attention is turning to the renewable energy sources. Photovoltaic (PV) solar energy is a direct conversion of solar radiation into electricity based on photovoltaic effect. It means the generation of a potential difference at the junction of two different materials in response to visible or other electromagnetic radiation by generating the electrons-holes [1]. PV technology and applications are characterized by their modularity – PV can be implemented on virtually any scale and size. The overall efficiency of systems available on the market varies between 6% and 15%, depending on the type of cell technology and application. The expected life span of PV systems is between 20 and 30 years. The solar modules are the most durable part of the system, with failure rates of only one in 10,000 per year. Some components, e.g. the inverter and battery, have to be replaced more regularly [2].

The major obstacle of using solar cells for electricity generation has been a much higher price when compared to the price of electricity generated from the traditional sources. There has been made a lot of efforts in the field of solar cells to reduce the price of solar electricity to a level that is comparable to the conventional electricity. The major cost in producing mc-solar cell panel is the wafer silicon production which is about 45 %, for material of module is about 35 % and 20 % for processing and assembling. So the cost reduction has been and is a key issue for solar cell application. The research and development of photovoltaic solar cell is aimed to increase efficiency, reduce yield loss, and decrease materials consumption. However, reduction of material consumption leads to thinner wafers, leading to a reduction of the mechanical stability of the wafers and increasing the number of broken wafers [1][3].

The photovoltaic industry needs to put an enormous pressure and optimization at every stage of the photovoltaic manufacturing chain of multicrystalline silicon wafer solar cell processing in order to reduce cost. One of the possible solutions is by reducing the thin of wafer for reducing the material consumption. However, this reduction leads to the reduced mechanical stability of wafer by increasing the number of broken wafers that reduces the yield of solar module. Optimization quality of silicon ingot as well as silicon wafer is possible to increase the mechanical stability of the wafer as well as efficiency of the solar cell. It can be

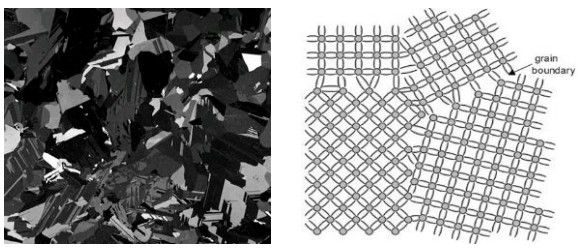
done through annealing treatment of the ingot in order to reduce the defect in the wafer [1][4][5].

1.2. Multicrystalline silicon

Silicon used for solar cells applications can be single crystalline, multicrystalline, or amorphous. In single-crystal silicon, the arrangement of crystal structure is uniform, because the entire structure is grown from the same crystal. Due to the manufacturing process is expensive which makes this type of silicon more expensive. Multicrystalline silicon contains several crystals and many grain boundaries are present. Manufacturing of mc-silicon is simpler which makes it cheaper than single crystalline silicon [2]. The multicrystalline silicon wafer have inhomogeneity and many types of defects such as grain boundaries, twin boundaries, dislocations, impurities and precipitates. These defects can have an impact not only on the diffusion length of minority charge carriers due to recombination processes, but also on the mechanical strength of the wafers [3][6].

Multicrystalline silicon can be produced by different methods. The most popular commercial methods involve a casting process in which molten silicon is directly cast into a mold and allowed to solidify into an ingot. The starting material can be refined lower-grade silicon, whereas higher-grade silicon is required for single-crystal material.

The material quality of multicrystalline material is lower than that of single crystalline material due to the presence of grain boundaries, as shown in figure 1. Grain boundaries introduce highly localized regions of recombination due to the introduction of extra defect energy levels into the band gap, thus reducing the overall minority carrier lifetime in the material. In addition, grain boundaries reduce solar cell performance by blocking carrier flows and providing shunting paths for current flow across the p-n junction. To avoid significant recombination losses at grain boundaries, grain sizes of the order of at least a few millimeters are required [1][2].



(a) (b)

Figure 1. (a).Multicrystalline silicon wafer;
(b). Boundary between crystals [2].

2. Processing of Multicrystalline Silicon Solar Cells

2.1. Silicon Wafer Preparation

Multicrystalline silicon is produced by a casting technique. Multicrystalline silicon rock is melted in a square crucible or melted in a separate crucible and then poured into the crystallization crucible. The cooling process must be well controlled to maintain a high quality of multi-crystal silicon as well as to provide a large grain size. The heat exchange process is a sophisticated procedure where the heat is locally extracted at the bottom of the crucible to produce course and homogeneous grains of silicon. The processing steps to produce a mc-silicon ingot are described in figure 2. [7].

The crucible material is commonly graphite, quartz coated with silicon nitride, or silica ceramic. Impurities such as carbon, oxygen and metal can be introduced in the multicrystalline ingot. The source of carbon impurities is from feedstock contamination and from carbon monoxide in furnace environments, which dissolves into the liquid silicon. Oxygen contamination is mostly dissolution of the quartz crucible into the silicon melt, which mainly influences the silicon ingot at the bottom. Metallic impurities come from the quartz crucible and its coating as well as from feedstock contamination [6] [2].

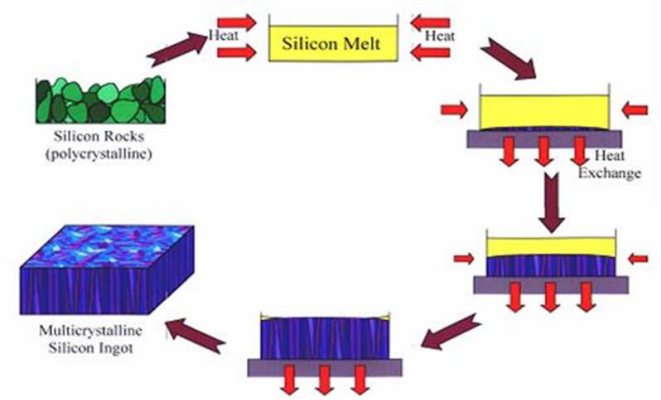


Figure 2. Multicrystalline silicon ingot growth process.

Impurities as well as defects should be neutralized as their presence is intrinsic to multicrystalline silicon wafers. Impurities like oxygen and metals are extracted by external gathering through phosphor diffusion during emitter diffusion. Immobile impurities should be passivated by interaction with hydrogen during the SiN:H anti reflection coating application. Hydrogen will diffuse into the bulk and make defects or impurities electrically inactive [7] [8].

2.2. Slicing the Multicrystalline Ingot

After growth, ingots should be cut by sawing off the edges of cylindrical ingots and further cutting into smaller blocks (brick) with the desire cross section. Silicon bricks are glued to a substrate holder and placed in a multi-wire saw that slices up the bricks into wafers as illustrated in figure 3[7].

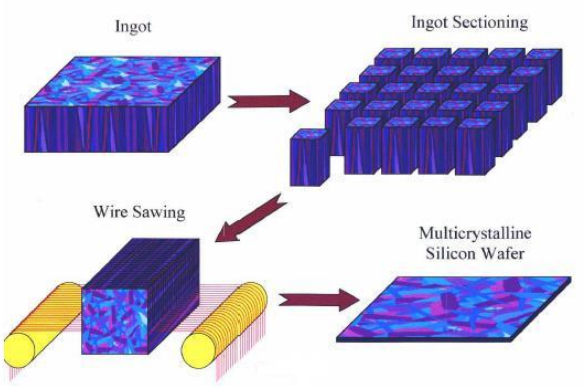


Figure 3. Sectioning ,slicing multicrystalline silicon ingot

Cutting is achieved by applying an abrasive slurry that usually consist of SiC over the wire webs, as shown in figure 4.

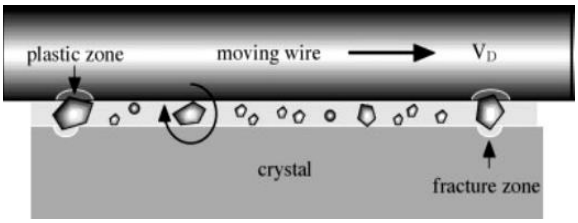


Figure 4. Schematic of wire slurry with abrasive and crystal in the cutting zone [7].

The interaction between the abrasive SiC particles and the crystal can induce local indentation creating microcracks as saw damage that penetrates around 10 μm deep into the wafer surface, as shown figure 5 [9].

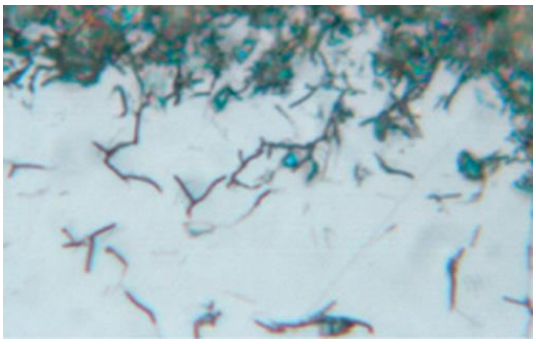


Figure 5. Cross section image of mc-silicon wafer after wire sawing.

This saw damage must be removed from the surface as well as from the edges of the wafer, because it reduces the mechanical strength of the wafer and increases recombination of charge carriers (electron-hole) in the surface region leading to a decrease in electrical efficiency. The sawing processes are induced of microcraks, which could be the origin of failures. The maximum depth of microcracks is related to many parameters such as slurry particle size, sawing load and sawing speed [10][5].

2.3. Etching and Texturing

1. Saw Damage Etching

Saw damage is removed through an etching process, which is done with a wet chemical process using alkaline and acidic solutions. Both types of etching solutions are used to remove shallow cracks at the surface and edges of the wafer. Alkaline etching is an anisotropic process where the etching rate will depend on the crystallographic plane so the etching rate will be different for different crystallographic orientations of multicrystalline silicon. On the other hand the acidic etching that uses a solution of HF, nitride acid (HNO_3) and water is an isotropic process, it is therefore better suited for saw damage removal and texturing of multicrystalline silicon. Both acidic etching and alkaline etching remove the shallow cracks and make them slightly shorter [7] [1].

In overall, it has been found that the length of a surface microcrack decreases as a result of the removal of the shallow part. If the initial crack is large enough, the crack can become wider as well as deeper after etching [7]. When saw damage etching is applied, around 10 μm of top surface layer is removed. The etched thickness also depends on the etching time. Generally etching can not remove the entire saw damage, because very deep surface cracks may still remain in the wafer. On the other hand, removal of a thicker surface layer by applying a longer etching time can create a groove at the grain boundaries. The sharp edge of this groove can serve as a starting point for crack propagation, which can reduce the strength of a mc-silicon wafer. One has to be very careful in choosing the etching time, as this is one of the main factors affecting the mechanical strength of silicon wafer and thus of solar cells.

2. Surface Texturing

Surface texturing is used to minimize light reflection. The wafers are textured to create a rough surface by producing a square-base pyramid surface structure for single crystalline silicon and worm like surface structure for multicrystalline silicon. The purpose of texturing is to increase the cell efficiency by increasing the chances of reflected light bouncing back onto the surface, rather than out to the

surrounding air [7]. Figure 6 represent the surface texturing principle.

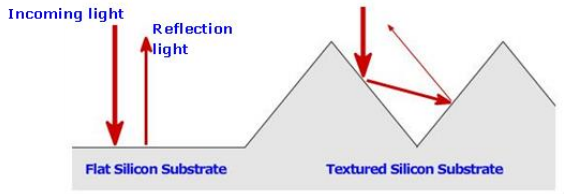


Figure 6. Surface texturing: reflected light can strike the silicon surface again thus reducing reflection.

Texturing is done via an etching process by altering the chemical solution concentration to more dilute. For single crystalline silicon wafer, this altered solution concentration leads to an increasing etching rate anisotropy, with the highest etching rate for the (100) plane and the lowest for the (111) plane. Single crystalline silicon wafers are ideal for texturing due to the correct crystal orientation for the formation of pyramidal etch structures having excellent anti-reflective properties. For multicrystalline wafers, the grain is randomly orientated, so only small fractions of grains are correctly oriented for texturing. This has led to an increase in the application of acidic etchants based on a HF:HNO_3 solution for the formation of texture, because acidic texturing gives a more uniform etch rate across grain boundaries [11]. The texture of single crystalline and multicrystalline silicon is shown on the figure 7.

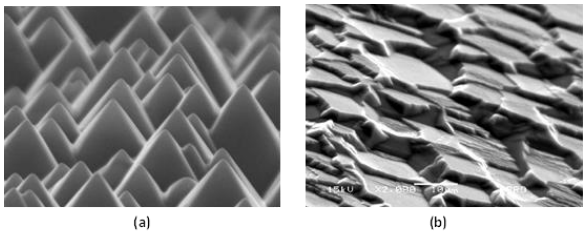


Figure 7.(a). SEM photograph of single crystal texturing. (b). SEM photograph of multicrystal texturing

Regarding the mechanical strength of multicrystalline silicon wafers, chemical etching will increase the mechanical strength of the wafer. By removing saw damage from the wafer the mechanical stability of the wafer tends to increase.

2.4. Phosphor Diffusion & Edge Isolation

1. Phosphor diffusion

Since the wafers are usually a moderately doped p-type of silicon with an acceptor concentration of 10^{16} cm^{-3} used as absorber, a highly doped n-type silicon layer on top of absorber is needed to create p-n junction. An n-type layer is generally created by phosphor diffusion in a diffusion furnace. The phosphorous atoms are diffused into silicon wafer at a temperature around 800 ºC - 1000 ºC to create an n-doped layer at the top of wafer (emitter). The thickness of this emitter layer is about 0.5 µm with a doping concentration > 2.10^{20} cm^{-3} [6]. An additional effect of phosphor diffusion is gettering of bulk impurities by diffusing it to the phosphor-rich layer (p-gettering), which improves bulk quality and as thus increase the efficiency. An illustration of phosphor diffusion is show in figure 8.

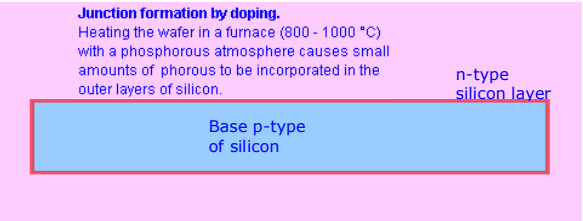


Figure 8. Phosphorus diffusion to form a p-n junction.

2. Edge Isolation

Phosphorus diffuses not only into the desired wafer surface, but it also extends into the side and opposite surface. This will give a shunting path between the cell front and rear. Removal of the path around the wafer edges as the edge junction isolation is commonly done by coin stacking the cells together. Stacked cells are placed into plasma etching chamber to remove edge isolation as illustrated in figure 9. Laser cutting is also a common technique for removing edge junction isolation.

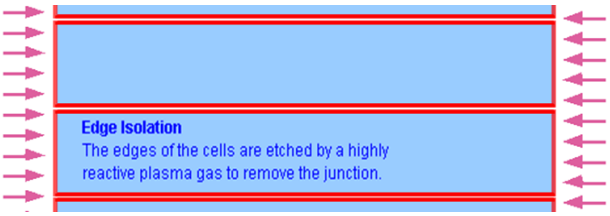


Figure 9. Removing edge isolation with plasma etching.

2.5. Silicon Nitride Deposition for Antireflection Coating

For textured multicrystalline silicon wafers, surface reflection is still high because the wafer surface is not textured well enough during the texturing process. Using an antireflection coating is essential to lower the light reflection. A layer of silicon nitride (SiN:H) is deposited onto the front side of the solar cell by using a chemical vapor deposition (CVD) technique. The thickness of silicon nitride (SiN_x:H) layer is about 70 – 80 nm [9].

Besides being an antireflection coating, SiN_x:H also functions to passivate the surface and the bulk. During annealing, hydrogen atom will diffuse into the silicon wafer as impurities, electrically inactive, thus improving the wafer quality [2] [12].

2.6. Metallization Process

1. Screen Printing of Ag front side

This technique is commercially available, robust, simple, and can easily be automated. The silicon wafer is moved on a conveyor belt to a printing table, as is illustrated in figure 10.

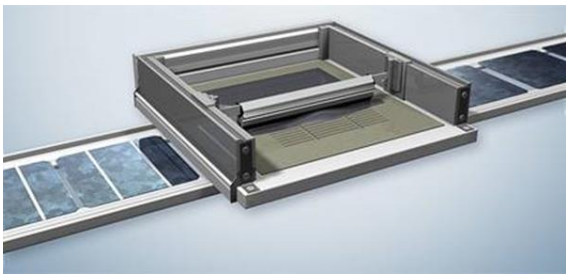


Figure 10. Screen printing process.

In order to make the silver (Ag) front contacts of solar cells, the metal paste normally consists of: 1) 70 wt% – 80 wt% of silver powder (Ag), 2) 1 wt%-10 wt% of lead borosilicate glass frit (PbO-B_2O_3-SiO_2) which serves to form the electrical contact and 3) 15 wt% - 30 wt% of organic component as solvent and binders. Some phosphorus compounds are added to dope underlying regions with more heavily n-type and for improving contact resistance [1]. The silver paste is forced through a pattern screen by dragging a squeegee across the screen as a result of which the silver paste is forced through holes in the screen print pattern. Those areas with gaps in the pattern leave a metal pattern on the surface of the wafer, as illustrated in figure 11.

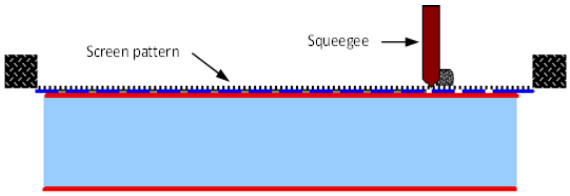


Figure 11. Front screen printing process.

2. Screen Printing of Al rear side.

The same screen printing equipment used for printing the Ag front side is applied for printing the Al rear side. Al paste is used for the formation of a good ohmic rear contact as well as an Al back-surface field (BSF) to p-type silicon by Al doping of the rear surface region during firing. A grid of silver is cheaper, but it does not produce a back surface field (BSF). Aluminum paste produces high performance cells with a BSF, but requires a second print of silver paste for solder-able contact [3].

The specimens with an Al layer show an increase in bending strength, possibly due to the formation of a eutectic layer (~12 % Si) and a BSF layer (1-2 x 10^{18} atom Al/cm^3 Si) at the outer fiber of the silicon wafer, as illustrated in figure 12. The maximum tensile stress in the silicon wafer will be located at the interface between the silicon wafer surface and aluminum bulk layer, i.e. in the eutectic and the BSF layer [1] [12].

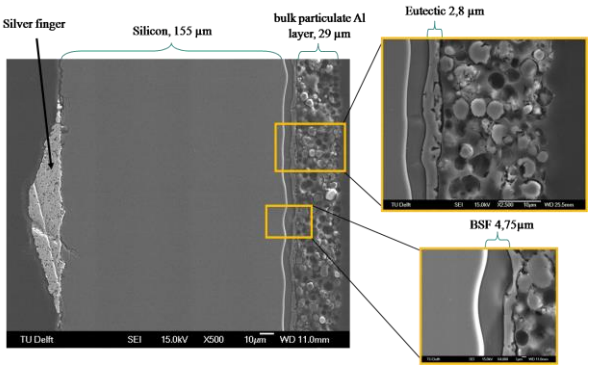


Figure 12. SEM images of the typical cross section of a solar cell with Ag layer, Si wafer and an Al back contact layer.

In order to give such suggestions, it is important to understand the microstructure of each layer. From previous investigations, it was found that the Al layer has a composite-like microstructure, consisting of three main components: 1) spherical hypereutectic Al-Si particles, 2) bismuth silicon glass and 3) porosity. However, as can be seen from the illustration in figure 13, the Al layer is not uniform and does not fully cover the eutectic layer, while the eutectic layer represent a uniform Al-Si bulk alloy, being 100 % in contact with BSF layer, and as a result with the silicon wafer [1] [8].

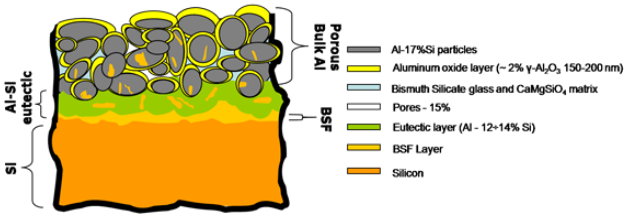


Figure 13. Microstructure model of Al back contact layer.

Since silicon is a very brittle material that exhibits linear elastic behavior, the presence of a 2nd ductile phase (i.e. the eutectic layer) could induce some plasticity at the outer fiber, thus altering the stress distribution and affecting possible crack initiation. Furthermore, this ductile phase (eutectic layer) can serve as a bridge for possible critical cracks at the silicon wafer surface itself, thus improving the strength of mc-silicon solar cells.

The amount of Al paste printed onto the rear side of the wafer is between 7-10 mg/cm^2 of dried Al paste. It is a very important parameter that can give an effect to the doping profile, thickness of the BSF, homogeneity, back surface reflectivity, and wafer bowing. Different thermal expansion coefficients (CTE) for aluminum and silicon (Al CTE of ~ 25x10^{-6} °C^{-1} and Si ~ 3.5x10^{-6} °C^{-1}) induce bowing of the wafer and forms a convex body during cooling process. Bowing starts to develop when the paste starts to resist the stresses generated due to the CTE mismatch. The amount of bowing at room temperature depends on: a) differences in CTE, b) the ratio of elastic modulii of the two materials, c) the ratio of thicknesses and, d) the temperature difference between the temperature at which coating becomes rigid and room temperature. Generally, bowing tends to decrease with reducing paste deposit amount but there is a practical lower limit below which screen-printed Al paste will result in a non-uniform back surface field layer. The wafer bowing becomes an issue when the Si wafer thickness is decreased below 240 µm; this can be related to the higher thickness ratio (thickness of Al / Si) [11] [12].

3. *Drying and Firing*

After the screen printing of front and rear sides with Ag and Al, the thick layer of wet metal paste is dried by heating to 250 °C – 400 °C in the oven in order to drive off organic solvent and binder. The electric contacts that are formed between wafer and metal paste are fired simultaneously in the firing furnace with a peak temperature around 850 °C to give reasonable metal resistivity [1]. Consequently, the contacts and conductive layers are imprinted in the cell within a furnace [12]. A simulated temperature profile for wafer firing is shown in figure 14, featuring a burn-out zone to burn organic binder and a sintering zone with a set peak temperature.

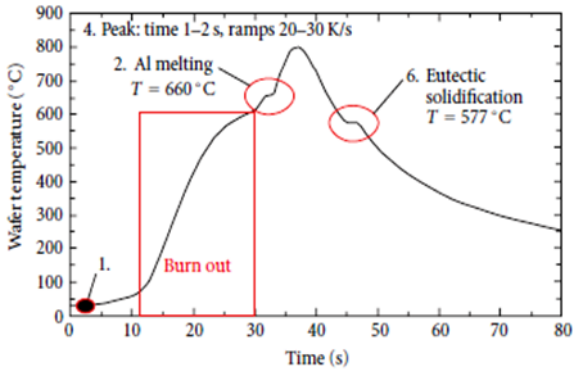


Figure 14. Temperature profile for firing Al paste in a belt furnace.

In the sintering zone, the front contact between silicon wafer and silver metal paste is formed by the process sequence: firing through silicon nitrate, formation of the Ohmic contact and contact sintering. In a similar way, the rear contact between silicon wafer and aluminum metal paste will form the back surface field, contact sintering, Ohmic contact and Al gettering. At the same time, the hydrogen of the SiN_x:H layer will release into the bulk of the wafer to passivate electrical defects.

The drying of aluminum paste is the 2nd step in order to drive-off organic solvent from the paste. After drying, a porous Al layer will cover the silicon wafer surface.

4. *Formation Al back surface contact*

Figure 16 explains in detail the model of screen printed rear contact formation [12]. Step 1 until 6 follow a description according to the number 1 – 6 in figures 16a and 16b.

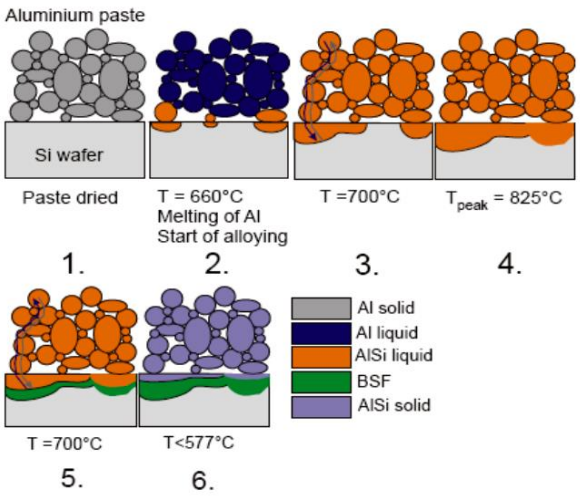


Figure 16. Model for formation of screen printed rear contact

A detailed explanation for point 1 – 6 in the figures 16 above is given below [1]: 1). Al paste consists of Al powder, a glass frit to enhance sintering, and organic binders and solvents. After drying, a porous paste matrix will cover the wafer surface. As the temperature is increased further the organic binder burns out; 2). The aluminum starts to melt at 660 °C which is visible as a small plateau in the temperature-time plot. The aluminum oxide Al_2O_3 surfaces of the Al particles stay in shape during the entire formation process. However, liquid Al penetrates through the Al_2O_3 surface locally and gets in contact with the wafer surface and other Al particles. The wafer surface is not yet fully covered with Al at this stage; 3). All aluminum paste particles will reach thermal equilibrium immediately after melting completely. At that time more and more silicon dissolves in the liquid aluminum as the temperature increases further. The volume of the Al

particles is limited by the Al_2O_3 skin and therefore stays constant. If Si gets dissolved in the Al particles, the same volume of Al is transported out of the particles onto the wafer surface; 4). At peak temperature, the entire wafer surface is covered with liquid Al-Si with exactly the same volume as that of the dissolved Si; 5). During cooling down, the (process no. 3) occurs in reversed direction, that is, Si is rejected from the melt to re-crystallize epitaxially on the wafer surface building up the Al-doped layer (Al BSF); 6). After reaching the eutectic temperature of 577 ℃, the remaining liquid phase solidifies instantly. The Al particles have the eutectic composition with 12 % of silicon dissolved and a certain amount of Al is found on the wafer surface between the BSF and the film of Al particles.

3. Conclusion

Multicrystalline silicon wafer is still the mainstay of most PV modules. Even the quality for produce electricity is still below the monocrystalline silicon due to inhomogeneity and present of defects but the mechanical properties is higher and producing cost is lower. Mechanical stability of silicon wafer became a serious issue due to reduction of wafer thickness, so probability for wafer to breakage is high; investigate the mechanism of wafer breakage is important to reduce breakage. The present of micro cracks reduces the mechanical strength of wafer significantly and wafer breakage will increase, because crack will start from the existing micro crack and that will propagate easier with presence of the stress. The photovoltaic industry needs to put an enormous pressure and optimization at every stage of the photovoltaic manufacturing chain in order to reduce cost. Every individual processing step for producing of multicrystalline silicon solar cell has an effect on mechanical stability. Mechanical stability is increase significantly after the etching process; on the other hand the screen printing process will reduce wafer strength over 30 %.

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